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1. Your reference — SP/4213 GB

2. Patent application number *(The Patent Office will fill in this part)* — 0307526.4

3. Full name, address and postcode of the or of each applicant *(underline all surnames)*

Council for the Central Laboratory of the Research Councils
Rutherford Appleton Laboratory
Chilton
Didcot
Oxfordshire
OX11 0QX

Patents ADP number *(if you know it)*

If the applicant is a corporate body, give the country/state of its incorporation — United Kingdom

8254088001

4. Title of the invention — ELECTRON MULTIPLIER ARRAY

5. Name of your agent *(if you have one)* — STEVENS HEWLETT & PERKINS

"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*

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Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

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8. Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'Yes' if:*

a) any applicant named in part 3 is not an inventor, or
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Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application.

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12. Name and daytime telephone number of person to contact in the United Kingdom SARAH PERKINS 0207 7404 1955

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ELECTRON MULTIPLIER ARRAY

The present invention relates to an electron multiplier array and to a method of making the same. In particular, the present invention is concerned with a compact, low power electron multiplier suited for use in, but not limited to, image intensifiers, flat panel displays and secondary electron emission microscopy.

Conventional electron multipliers, in the form of a photomultiplier tube for example, are constructed using a plurality of electrically conductive plates, with each plate having high secondary electron emission characteristics. The conductive plates are individually mounted in a vacuum chamber in a column but physically separated from one another and an anode is provided at one end of the column. The conductive plates are connected to a power source such that increasingly positive potentials are applied to successive plates in the column in a direction towards the anode whereby free electrons are caused to accelerate towards the anode at the base of the column. When an electron is incident on the first plate in the column, distant from the anode, a plurality of electrons is produced by the plate because of its high secondary electron emission. The electrons produced by the first plate are then accelerated towards the anode and in turn are incident on the next plate. Thus, ever increasing numbers of electrons are emitted by each of the plates as the electrons are accelerated towards the anode at the base of the column, in a cascade.

In an article appearing in Nuclear Instruments and Methods in Physics research A 3443 (1994) 263-267 entitled 'Status of the Ceramic Multichannel PM tube' G Comby et al, a photomultiplier array is described which is constructed from individual ceramic plates that are stacked alternately as dynode layers and insulation layers. A plurality of holes is drilled into each ceramic plate and the ceramic plates are stacked so that the holes in adjacent plates are in staggered alignment. The walls of the holes in the dynode plates are lined with a conductive material that is in electrical contact with an applied positive potential so that electrons in the channel defined by the holes are accelerated towards an anode at the base of the stack.

Conventional electron multiplier devices of the type described above, have the disadvantages that the devices are bulky and are susceptible to high magnetic fields which significantly reduces potential applications for such devices. Moreover, the method of making the devices is costly and time consuming. Each plate must be manufactured separately and when the plates are stacked care must be taken to ensure the necessary staggered arrangement.

In WO99/09577 an electron multiplier array is described in which alternating insulation and dynode layers are built up from a substrate, around an array of anodes, using conventional deposition and etching techniques. The method of manufacture of the electron multiplier array employs silicon dioxide as the material insulating the individual dynodes from one another and requires the dynodes to be deposited directly on the exposed upper surface of the silicon dioxide. Resist is used to fill the channels of the multiplier that are formed as each new layer is deposited. Once the multiplier stack is complete, the resist is then removed to provide continuous staggered channels from the upper surface of the multiplier array to individual anodes at the base of each channel.

The multiplier array described in WO99/09577 is particularly suited to pixellated sensing and imaging. However, to ensure comparative outputs from the individual channels of the array, the performance of each channel must be measured and appropriate correction factors applied to the channel outputs as small variations in the thicknesses of a layer across channels can alter the relative performance characteristics of the channels.

The present invention seeks to provide an improvement over the method of fabricating an electron multiplier array as described in WO99/09577 and to provide an improved electron multiplier array which reduces and ideally eliminates the need for individual channel outputs to be corrected for variations in performance.

In a first aspect the present invention provides an electron multiplier array comprising a monolithic structure comprising a plurality of alternately stacked layers of a metallic material and an insulator there being an array of open channels extending through the layers of metallic material and the layers of insulator, each of the metallic layers having a respective power connection

for application of a voltage potential which varies with respect to the location of the metallic layer within the stack, the electron multiplier array being further characterised by a plurality of planarising layers each planarising layer separating neighbouring insulator and metallic layers in the stack.

In a second aspect the present invention provides an electron multiplier array comprising a monolithic structure having a plurality of alternately stacked layers of a metallic material and an insulator there being an array of open channels extending through the layers of metallic material and the layers of insulator, each metallic layer consisting of a plurality of discrete but interconnected cells, each cell defining the walls of a respective channel and each cell being connected to a plurality of adjacent cells in said layer and each of the metallic layers having a respective power connection for application of a voltage potential which varies with respect to the location of the metallic layer within the stack, the power connections for each of the metallic layers being located at different respective positions on the perimeter of the electron multiplier array.

In a preferred embodiment the alternately stacked layers of metallic material and insulator are mounted on a substrate which closes one end of the channels of the array and includes an anode at the closed end of each channel of the array.

In an alternative preferred embodiment in which the electron multiplier array is suitable for use as part of an image intensifier, a first, upper surface of the array may be provided with or located adjacent a photosensitive material and a second, opposite end of the array may be located adjacent a phosphor surface.

In a further aspect the present invention provides a method of manufacturing a monolithic electron multiplier array comprising the steps of:

a) providing a substrate;

b) depositing a layer of insulator;

c) patterning an array of apertures in the layer of insulator;

d) introducing a filler material into the array of apertures in the layer of insulator;

d) applying a planarising layer over the exposed surfaces of the layer of insulator and the filler material in the apertures;

e) applying a layer of a metallic material over the planarising layer;

f) forming an array of apertures in the layer of metallic material, the apertures in the layer of metallic material defining with the filled apertures in the layer of insulator respective channels in the monolithic structure;

g) introducing a filler material into the array of apertures in the layer of metallic material;

h) applying a planarising layer over the exposed surfaces of the layer of metallic material and the filler material in the apertures;

i) repeating the steps b) to h) to form alternately stacked layers of a metallic material and insulator with an array of channels extending through the layers of metallic material and the layers of insulator; and

j) removing the regions of each planarising layer overlying filler material and the filler material in the apertures in each layer so as to from an array of open channels extending through the alternately stacked layers of metallic material and insulator.

Embodiments of the present invention will now be described by way of example with reference to the accompanying drawings, in which:

Fig. 1 illustrates a single channel of an electron multiplier array in accordance with the present invention;

Figs 2A –2K illustrate the stages of a fabrication method of the electron multiplier array of Fig. 1; and

Fig. 3 is a plan view from above of the power connections for one dynode layer in the electron multiplier array of Fig. 1.

The monolithic electron multiplier 1 of Fig. 1 generally comprises a substrate 2, of intrinsic silicon for example, on which is mounted an anode 5 and an alternative series of insulation layers 7 and dynode layers 11. Each dynode layer is of an electrically conductive, preferably metallic, material and has its exposed surfaces coated with a material having high secondary emission characteristics. For the sake of clarity only a portion of the total number of secondary electrons that may be generated within one channel of the electron multiplier are illustrated. Each layer is separated from its closest neighbours by a planarising layer 10 in the form of a thin film of a metallic material, preferably the same material as the material of the dynode layers.

Each layer has an aperture through the layer which communicates with the apertures in the layers above and below so as to define a continuous channel from the upper surface of the multiplier to the anode 5 at the base of the channel. However, the apertures in successive dynode layers are arranged so as to be partially offset from each other thereby describing a repeating S-shaped path to the anode 5. It is to be understood that although the illustrated embodiment includes an anode located at the end of the channel, the same general structure may be implemented as a micro-channel plate in which case the anode is omitted and the supporting substrate may be back-etched after fabrication.

The electron multiplier 1 of Fig. 1 is preferably fabricated in accordance with the following method. An array of microlenses 3 are lithographically defined on a substrate 2 such as a silicon wafer. Only one microlens is illustrated in Figs 2A through 2K. The microlenses 3 are of a thermally deformable plastics material such as those available under the trade mark QUDOS which adopt a generally convex shape following exposure to heat (Fig. 2A). By using a microlens as the supporting structure of the anode, a smooth dome-shaped external anode surface is achieved. This minimises the risk of secondary electron emission from the anode itself.

A thin film 4 of a chrome:gold alloy is then deposited over the convex surfaces of the microlenses 3 and the exposed surface of the substrate 2 (Fig. 2B). The alloy film 4 preferably has a thickness between 0.05-4 microns in thickness, more preferably 0.1-1 microns. To ensure the alloy film 4 is clearly visible, in Figures 2A through 2K the thickness of the alloy film 4 is greater than the ranges of thicknesses mentioned above. The thin alloy film 4 is then patterned leaving the convex surface of each microlens 3 covered by the alloy to form an array of anodes 5. Each of the anodes 5 also has a power supply connection 6 in the form of a thin strip of the alloy film (Fig. 2C). Ideally, the anodes 5 are arranged in a regular grid structure with a spacing of between 10 and 500 microns, preferably less than 100 microns. However, the arrangement of the anodes and their associated multiplier channels can be varied subject to the requirements of a particular application of the multiplier array.

A first insulation layer 7 of preferably 10 microns is then applied over the surface of the substrate and the anodes 5 through a mask (not illustrated). The first insulation layer 7 is patterned by the mask so as to provide a plurality of apertures 8 each in the form of a channel aligned with and exposing a respective anode 5 (Fig. 2C). Each aperture 8 is preferably around 10 microns in diameter, although diameters of ranging from 5 to 50 microns are envisaged. The aperture 8 may be substantially circular thereby describing a substantially continuous aperture wall or the wall of the aperture 8 may be discontinuous and have a more complex structure, for example a six-sided structure, for reasons of structural integrity and / or minimising use of material amongst others.

The insulation layer 7 is preferably an insulating material such as Cyclotene™ or other similar insulating materials which can be deposited, etched and planarised using conventional techniques. In the case of Cyclotene™, the material may be either spin or spray coated onto the exposed upper surface of the substrate, under the conditions recommended by the manufacturer. Conveniently, as long as the thickness of the insulation layer 7 is at least approximately three times the thickness of the alloy film, in spin / spray coating the Cyclotene™ the insulation layer should automatically be approximately planarised. Thereafter, the structure of the channel is photodefined in the Cyclotene™ and the channel dry etched using a fluorine based plasma, for example.

A filler material 9, such as a polyimide, is then deposited into the apertures 8 so as to completely fill the apertures and extend over the exposed upper surface of the insulation layer 7 (Fig. 2D) Preferably, the filler material 9 is a low outgassing, thermally cured material such as a conventional photoresist which is suitable for oxygen plasma etching. The filler material 9 is preferably spin or spray coated over the insulation layer and into the apertures 8. Ideally, the filler material is thermally curable at temperatures preferably below 250°C, although where Cyclotene™ is used as the insulation layer, filler materials may be employed having curing temperatures as high as 300 – 350 °C.

The filler material 9 above the surface of insulation layer 7 is [illegible] as to subsequently removed, preferably by means of plasma etching, to expose the surface of the insulation layer 7. Next, a [illegible]ous seed layer 10 in the form of a thin film of an alloy such as chrome:copper is deposited over the exposed surface of the insulation layer 7 and the filler material 9 (Fig. 2E). The seed layer 10 is preferably deposited using conventional electroplating techniques and acts as a plating layer for the structure being fabricated. The thickness of the plating layer preferably ranges between 0.05 and 0.5 microns depending upon the specific composition of the alloy.

As illustrated in Fig. 2F, a dynode layer 11 is then deposited over the seed layer 10 through a mask (not illustrated). The dynode layer 11 is preferably an electrically conductive, metallic material and ideally is of the same alloy as the seed layer, e.g. chrome:copper, and is deposited to a thickness of between 1-20 microns, more preferably approximately 10 microns with the precise thickness being dependent upon the desired diameter of the aperture to be provided through the dynode layer 11. By means of the mask, the dynode layer 11 is patterned with a plurality of apertures 12 each aperture being associated with a respective anode 5 beneath. For this lowermost dynode layer, the array of apertures 12 is preferably arranged with the axis of each dynode aperture 12 offset from the axis of its associated anode 5 that lies beneath, as shown in Fig. 1. Alternatively, as illustrated in Fig. 2F, the apertures 12 in the dynode layer 11 may be smaller in diameter than the apertures through the insulation layer 7 but aligned with the axis of the respective anode 5. In either case this structure results in an edge of the dynode aperture overhanging the anode 5.

As illustrated in Fig. 3, instead of a continuous layer of alloy in which an array of apertures are provided, the structure of the dynode layer 11 may be patterned as a series of discrete but interconnected cells which the inner wall of each cell defining a single channel aperture. With this structure, the interconnections between the cells act as power connections to apply the voltage potential across the dynode layer. As each dynode cell has multiple interconnections, as is discussed later in this document, these connections may be fusable to enable the array to work even where some of the channels of the array are defective. Although the dynode cells are illustrated as rings, it

course be apparent that alternative interconnected structures each defining ective channel aperture may be adopted.

The aper 12 in the dynode layer 11 are then filled with the same filler material 13 which w eposited in the lower aperture in the insulation layer 7 (Fig. 2G). The filler mat 13 is deposited so as to wholly fill the apertures 12 and extend over the expo upper surface of the dynode layer 11. Thereafter the filler material 13 is remove back to the upper surface of the dynode layer 11 and a new seed layer 10 is dep ited over the exposed surface of the dynode layer 11 and the filler material 13 in each of the dynode apertures 12 (Fig. 2H). The new seed layer 10 is again preferably of the same metallic material as the dynode layer and is preferably continuous across the entire upper surface of the device.

The fabrication steps described above are then repeated to create an alternating series of insulation and dynode layers with each layer being isolated from its adjacent layers by continuous thin films acting as seed layers (Fig. 2I-2J). The seed layers ensure that each layer in turn is planarised across the surface of the device thereby minimising any variation in the thickness of each layer across the device.

Each layer includes an array of apertures which are filled with the filler material and which are arranged so that the apertures in successive dynode layers are not concentric with one another and instead are partially offset from the channel apertures in the dynode layers above and below so as to define a staggered channel from the uppermost layer to the anodes 5 at the bottom of the channels. Preferably, the offset arrangement of the apertures in adjacent dynode layers is achieved by employing the same mask for the deposition of each dynode layer but adjusting the position of the mask for each layer, for example by rotation of the mask. An alignment key 14 (Fig. 1) may be provided adjacent the edge of the substrate with which the mask can be aligned in at least two different positions. As illustrated in Fig. 1 it is not necessary for the apertures in the insulation layers to be offset from one another. Instead the apertures in the insulation layers 7 may be concentric with one another.

Once all of the insulation and dynode layers have been completed, a final upper seed layer 10 is deposited so as to planarise the uppermost

dynode layer 11. At least part of the seed layer 10 is thereafter removed so as to expose the filler material in the apertures 12 of the uppermost dynode layer 11. The filler material is then removed, for example by means of plasma etching, to open the apertures 12 in the dynode layer 11 and to expose the seed layer 10 beneath. Part of this lower seed layer 10 is also then removed to expose the filler material in the apertures 8 in the adjacent insulation layer 7. The filler material in the insulation layer apertures 8 is then removed to expose the next seed layer 10 and that exposed seed layer 10 is in turn etched so as to expose the filler material beneath. Removal of this seed layer 10 may additionally result in exposed surfaces of the dynode layer 11 being partially etched. However, this is not a problem as the dynode layer 11 is considerably thicker than the adjacent seed layers 10. The process of removing the filler material in the apertures of both the insulation layers 7 and the dynode layers 11 and the exposed regions of the seed layers 10 is then repeated through each of the layers until the anode 5 at the base of each one of the channels is exposed (Fig. 2K).

Once all the filler material has been removed the walls of the channels are cleaned so as to remove any copper oxide that has formed and then the exposed surfaces of each of the dynodes or at least the active surfaces of each of the dynodes are coated with a secondary emissive material such as oxidised beryllium copper or caesiated antimony 15.

Finally, each dynode layer is provided with power supply connections so that a voltage potential may be applied between each dynode layer. Also, the substrate is preferably mounted on a ceramic substrate and the array of anodes is provided with connections to output signals to a signal analyser (not illustrated).

The electron multiplier array described above may be implemented in various devices including but not limited to image intensifiers, flat panel displays and secondary electron emission microscopes.

In the case of an image intensifier, as mentioned earlier, the electron multiplier may be fabricated with the anode at the base of each channel replaced by a phosphor screen. Preferably, for this particular application the array of electron multiplier tubes is fabricated on the silicon substrate in the manner described above and thereafter the substrate is removed by etching

to open the ends of the channels which are then aligned with a separate phosphor screen. To provide the necessary sensitivity to incident photons, the upper surface of the array of electron multiplier tubes may be coated with a photosensitive material and to prevent the photosensitive material from penetrating the channels, the evaporation source is preferably offset from the surface of the array and the array is rotated to ensure even coverage of the photosensitive material. Alternatively, the array of multiplier tubes may be aligned behind a glass window which is coated on its inner surface with a photosensitive material. The photosensitive material is selected in dependence on the wavelengths of light to be detected such as, but not limited to, bialkali materials.

Finally, for certain applications the electron multiplier array may be mounted in an enclosure which is evacuated and sealed with a window of quartz or glass. The window may be backed with a thin film of indium-tin-oxide (ITO) so that a potential may be applied to the window without affecting its transparency.

Considering the preferred structure of the dynode layers in the form of discrete but interconnected cells, and the high voltage potentials that are applied to the individual dynode layers, as illustrated the voltage connections to each of the dynode layers can be arranged at respective unique positions about the edge of the structure. Preferably, as illustrated, for the sake of convenience the voltage connections 16 are arranged adjacent one another but at different circumferential positions. Although the multiplier array of Figure 3 has a circular periphery it will be immediately apparent that the periphery of the array may be any shape.

By providing planarising layers at a plurality of intermediate depths through the multiplier structure, the thicknesses across the array of individual layers are maintained thereby contributing to consistent, and comparative, performance characteristics of the individual channels of the array. Furthermore, the large number of individual channels and the very small size of the channels mean that the electron multiplier array is capable of performing extremely high resolution imaging. The smaller dimensions also mean that the array is able to tolerate much higher magnetic fields than conventional devices. Moreover, the array is resistant to ionising radiations

and temperature variations that can undermine conventional semiconductor devices.

The electron multiplier array described above may have a surface area of many square centimetres in which thousands of individual electron multiplier channels are formed. This means that in many cases failure of a few of the individual channels in the array may not undermine the overall performance or effectiveness of the device, as long as failure of individual channels does not result in failure of the whole array. Such failures may arise during fabrication or as a result of a foreign particle entering a channel. As described earlier the interconnection of the dynodes as illustrated in Fig. 3, or using a similar arrangement of multiple dynode interconnections, enables the connections around a fused channel to be shorted without causing damage to the connections of the other channels. In this way a system is provided for disabling and isolating damaged channels to permit continued use of the photomultiplier array by selection of the supply current to match the fusing limit. Thus, for the illustrated embodiment where a single channel in the array is shorted then the maximum current will flow through the connections to the dynode rings of that channel whereas the connections to dynode rings of functioning electron multiplier channels are subjected to only a third of the maximum voltage. Thus, by careful selection of the applied current to that dynode layer the connections to a defective channel may be fused.

The electron multiplier array described herein and its applications are not limited to the details of the embodiment described herein and instead is limited only to the spirit and scope of the accompanying claims.

CLAIMS

1. An electron multiplier array comprising a monolithic structure comprising a plurality of alternately stacked layers of a metallic material and an insulator there being an array of open channels extending through the layers of metallic material and the layers of insulator, each of the metallic layers having a respective power connection for application of a voltage potential which varies with respect to the location of the metallic layer within the stack, the electron multiplier array being further characterised by a plurality of planarising layers each planarising layer separating neighbouring insulator and metallic layers in the stack.

2. An electron multiplier array comprising a monolithic structure having a plurality of alternately stacked layers of a metallic material and an insulator there being an array of open channels extending through the layers of metallic material and the layers of insulator, each metallic layer consisting of a plurality of discrete but interconnected cells, each cell defining the walls of a respective channel and each cell being connected to a plurality of adjacent cells in said layer and each of the metallic layers having a respective power connection for application of a voltage potential which varies with respect to the location of the metallic layer within the stack, the power connections for each of the metallic layers being located at different respective positions on the perimeter of the electron multiplier array.

3. An electron multiplier array as claimed in either of claims 1 or 2, wherein the alternately stacked layers of metallic material and insulator are mounted on a substrate which closes one end of the channels of the array.

4. An electron multiplier array as claimed in claim 3, wherein an anode is provided at the closed end of each channel of the array.

5. An electron multiplier array as claimed in claim 4, wherein each anode comprises a microlens coated in a thin metallic film.

6. An electron multiplier array as claimed in any one of the preceding claims, wherein for each channel of the array the edges of the apertures in each layer of metallic material defining the channel partially overlap the aperture edges in neighbouring metallic layers for the same channel.

7. An electron multiplier array as claimed in any one of the preceding claims, wherein the layers of metallic material consist of an alloy of chrome and copper.

8. An electron multiplier array as claimed in any one of the preceding claims, wherein the active surfaces of each metallic layer are coated in a high secondary emissive material.

9. An electron multiplier array as claimed in claim 8, wherein the secondary emissive material is selected from oxidised beryllium copper and caesiated antimony.

10. An electron multiplier array as claimed in any one of the preceding claims, wherein the layers of insulator consist of a dry-etchable material.

11. An electron multiplier array as claimed in claim 1, wherein the material of the planarising layers and the metallic layers is the same.

12. A method of manufacturing a monolithic electron multiplier array comprising the steps of:

a) providing a substrate;

b) depositing a layer of insulator;

c) patterning an array of apertures in the layer of insulator;

d) introducing a filler material into the array of apertures in the layer of insulator;

d) applying a planarising layer over the exposed surfaces of the layer of insulator and the filler material in the apertures;

e) applying a layer of a metallic material over the planarising layer;

f) forming an array of apertures in the layer of metallic material, the apertures in the layer of metallic material defining with the filled apertures in the layer of insulator respective channels in the monolithic structure;

g) introducing a filler material into the array of apertures in the layer of metallic material;

h) applying a planarising layer over the exposed surfaces of the layer of metallic material and the filler material in the apertures;

i) repeating the steps b) to h) to form alternately stacked layers of a metallic material and insulator with an array of channels extending through the layers of metallic material and the layers of insulator; and

j) removing the regions of each planarising layer overlying filler material and the filler material in the apertures in each layer so as to from an array of open channels extending through the alternately stacked layers of metallic material and insulator.

13. A method as claimed in claim 12, wherein each planarising layer is applied as a continuous layer extending over substantially all of the exposed upper surface of the array.

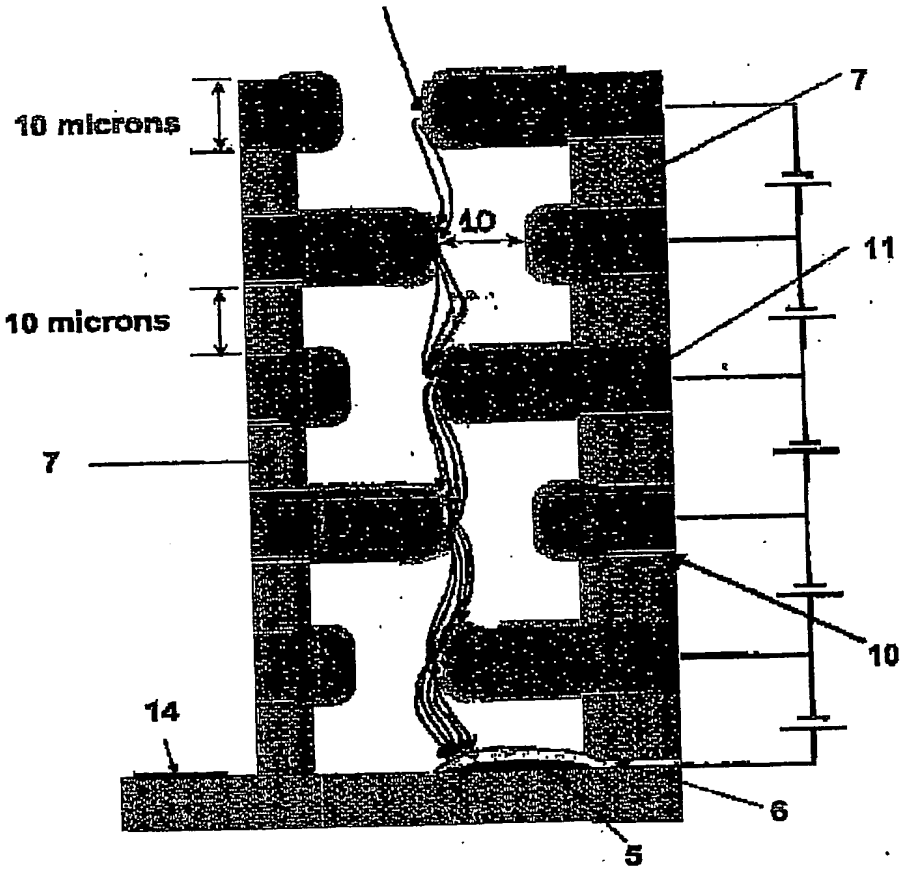


Fig. 1

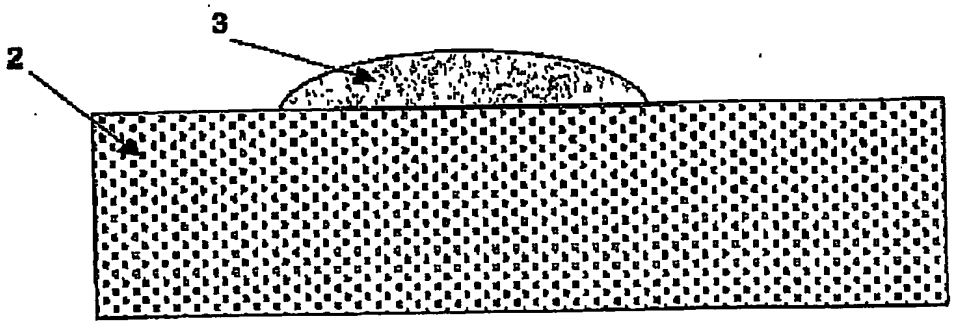


Fig. 2A

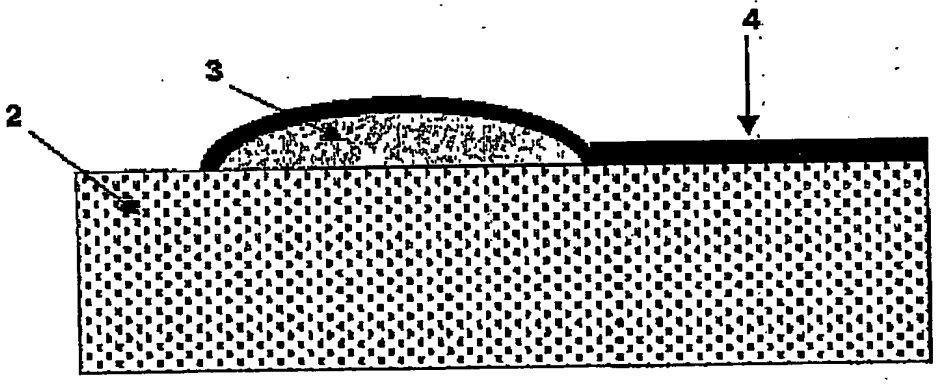


Fig 2B

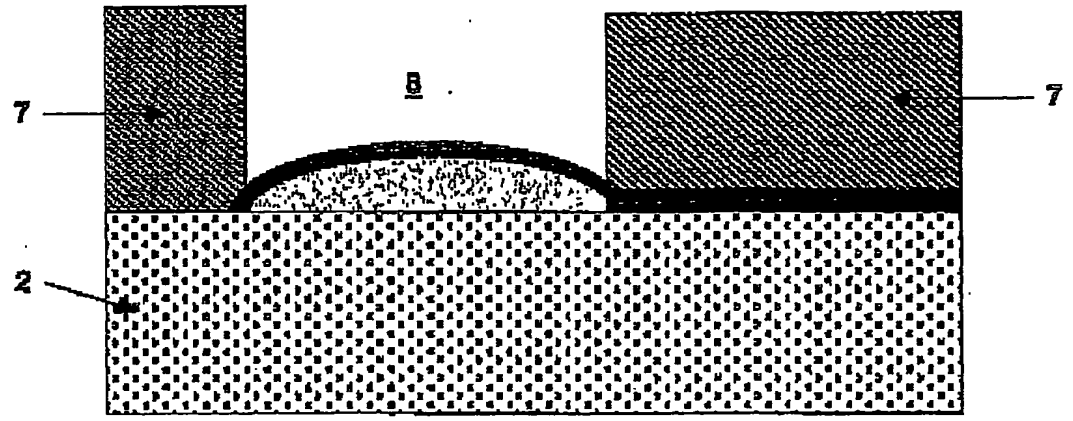


Fig. 2C

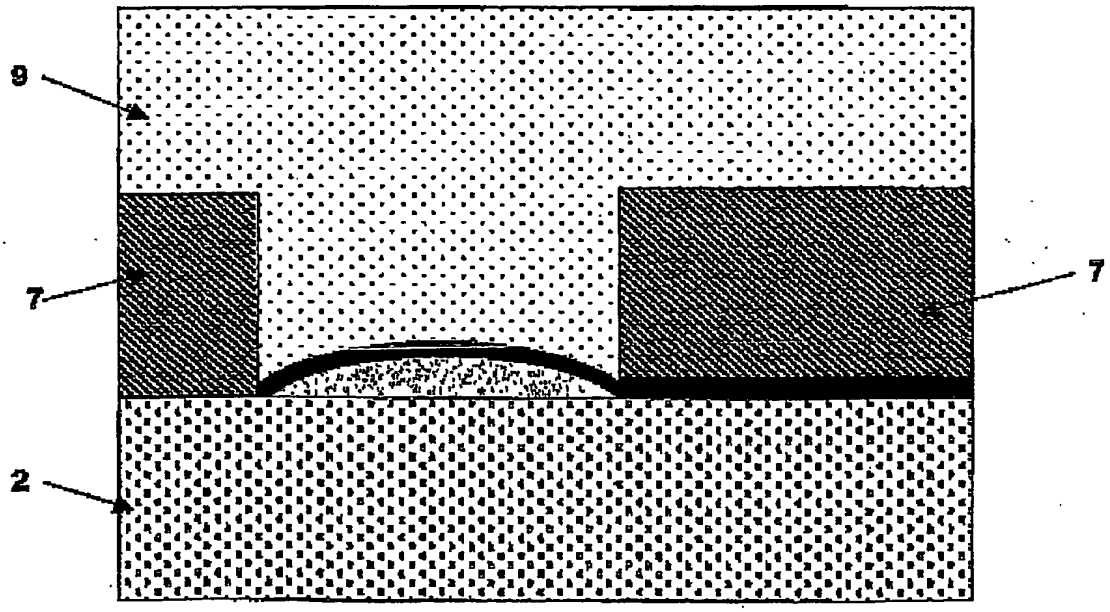


Fig. 2D

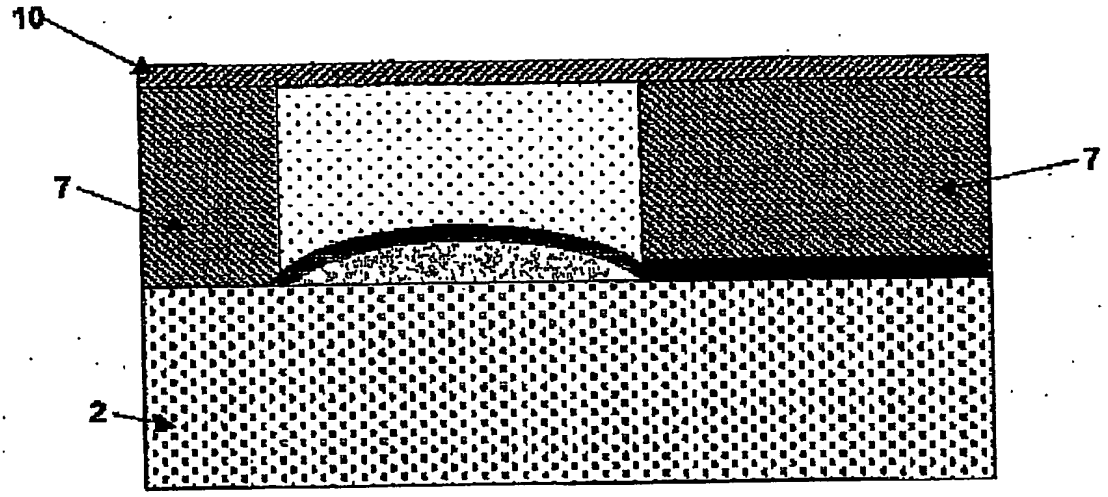


Fig. 2E

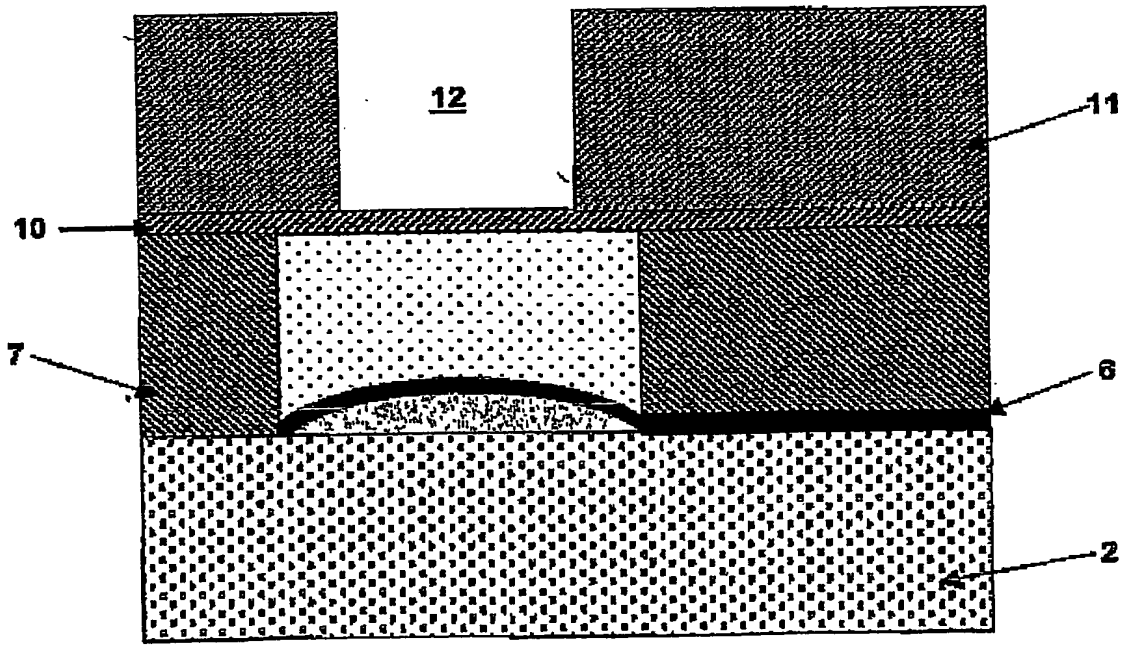


Fig. 2F

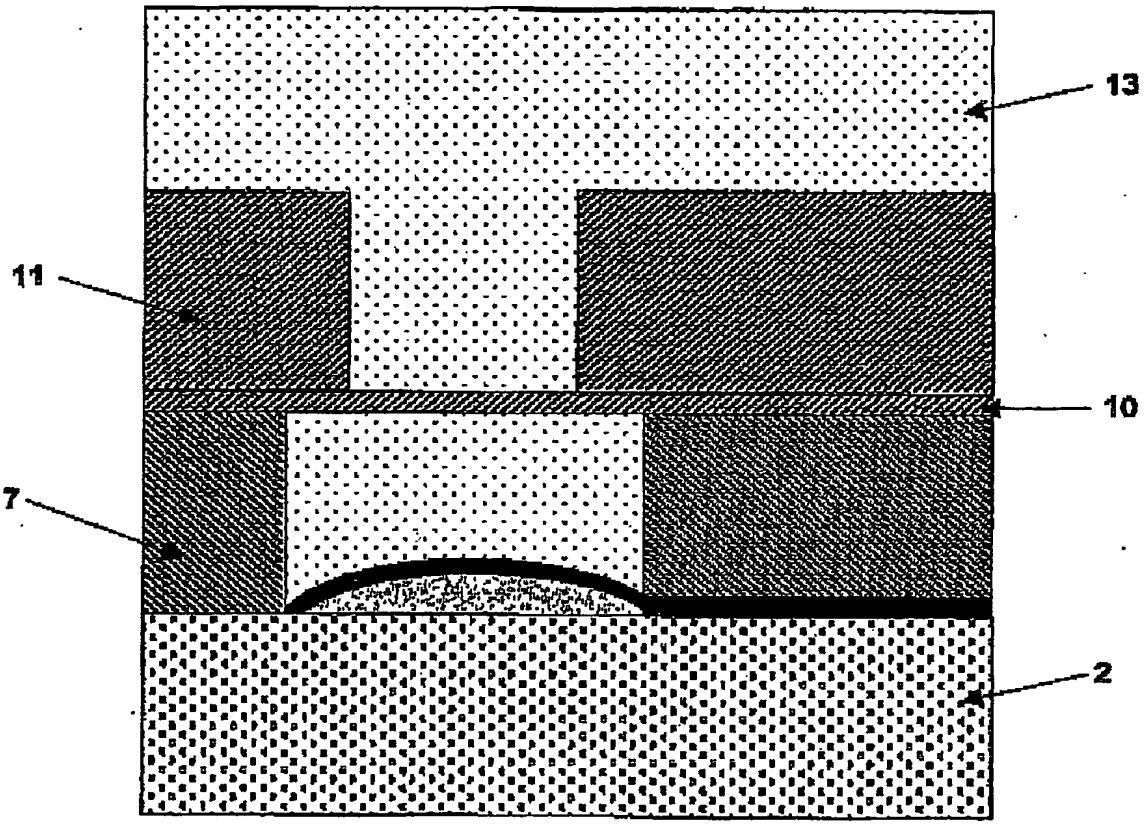


Fig.2G

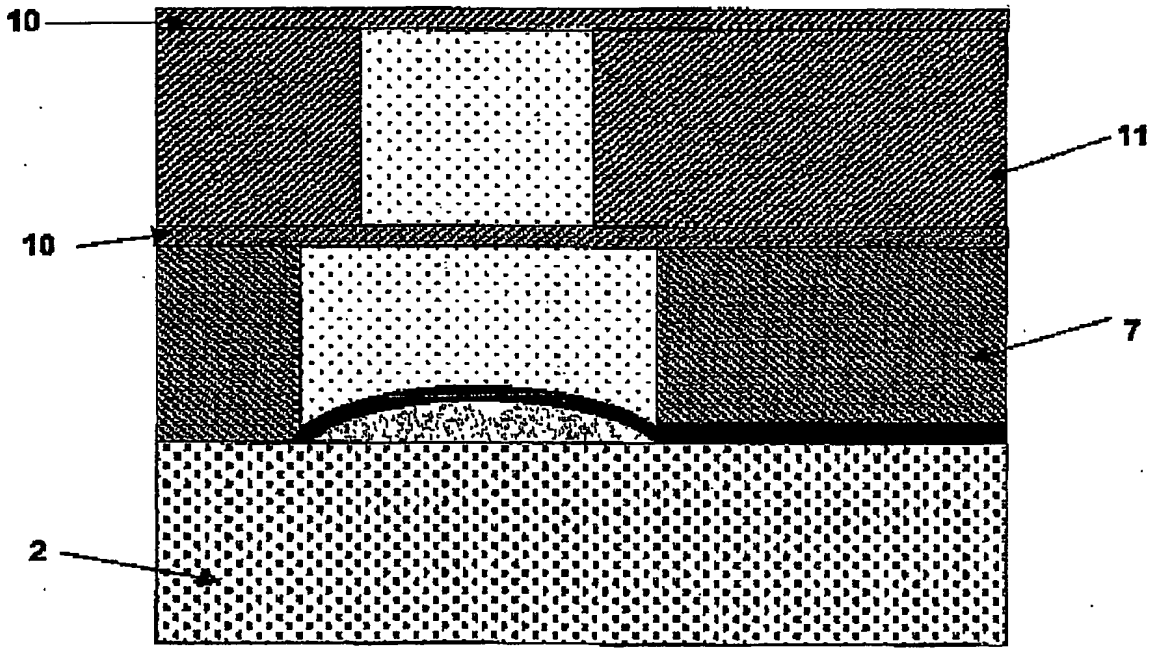


Fig. 2H

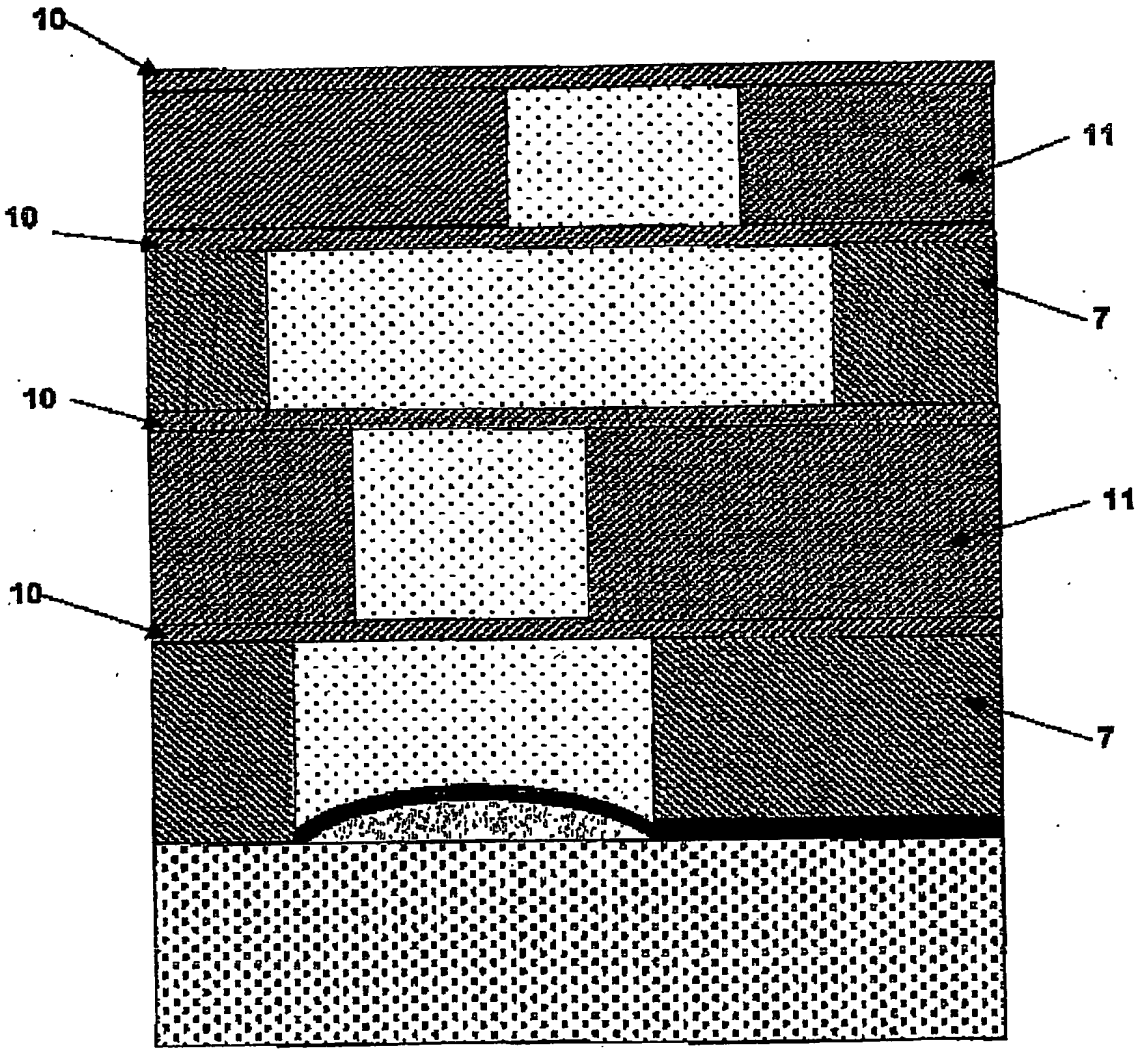
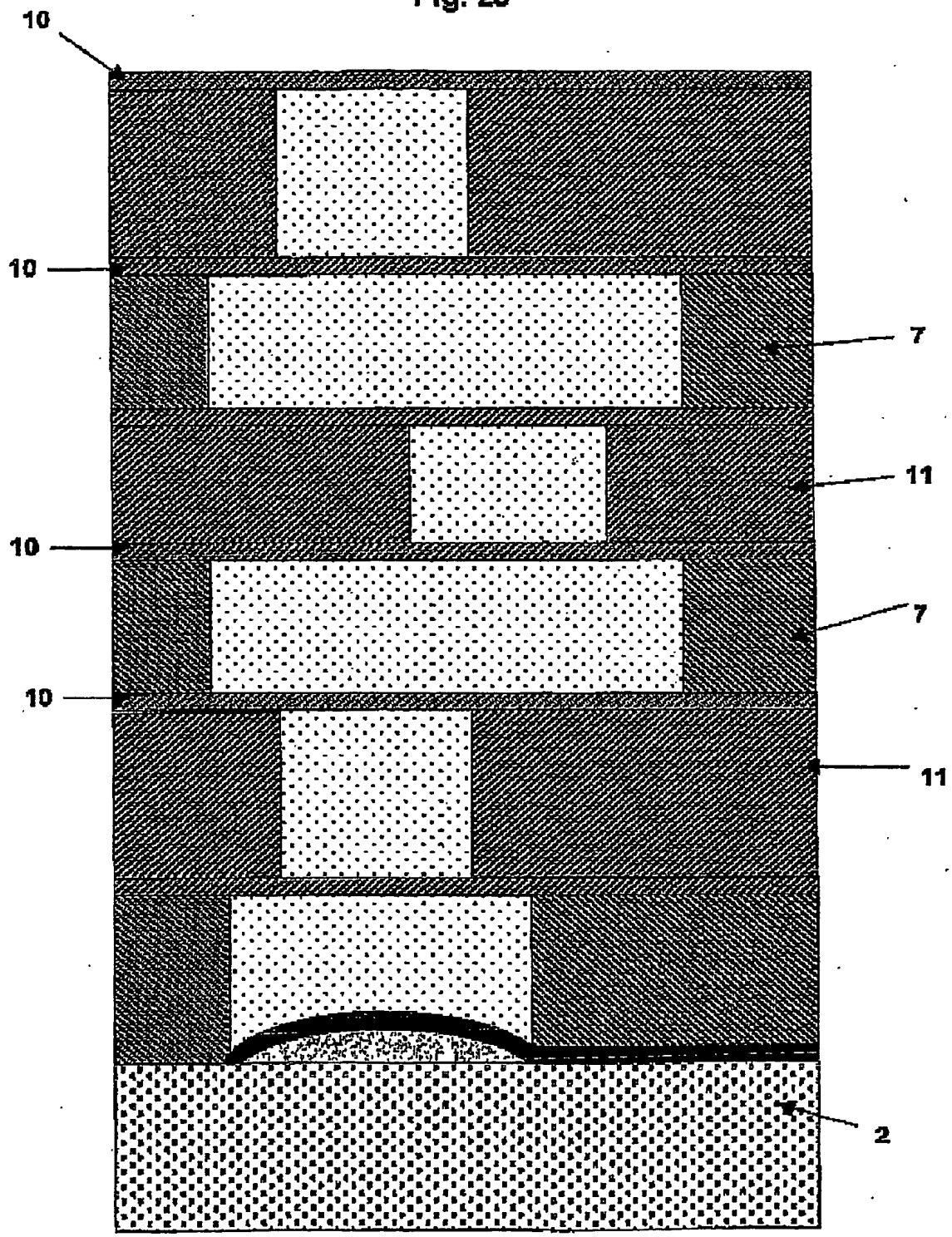


Fig. 2l

Fig. 2J



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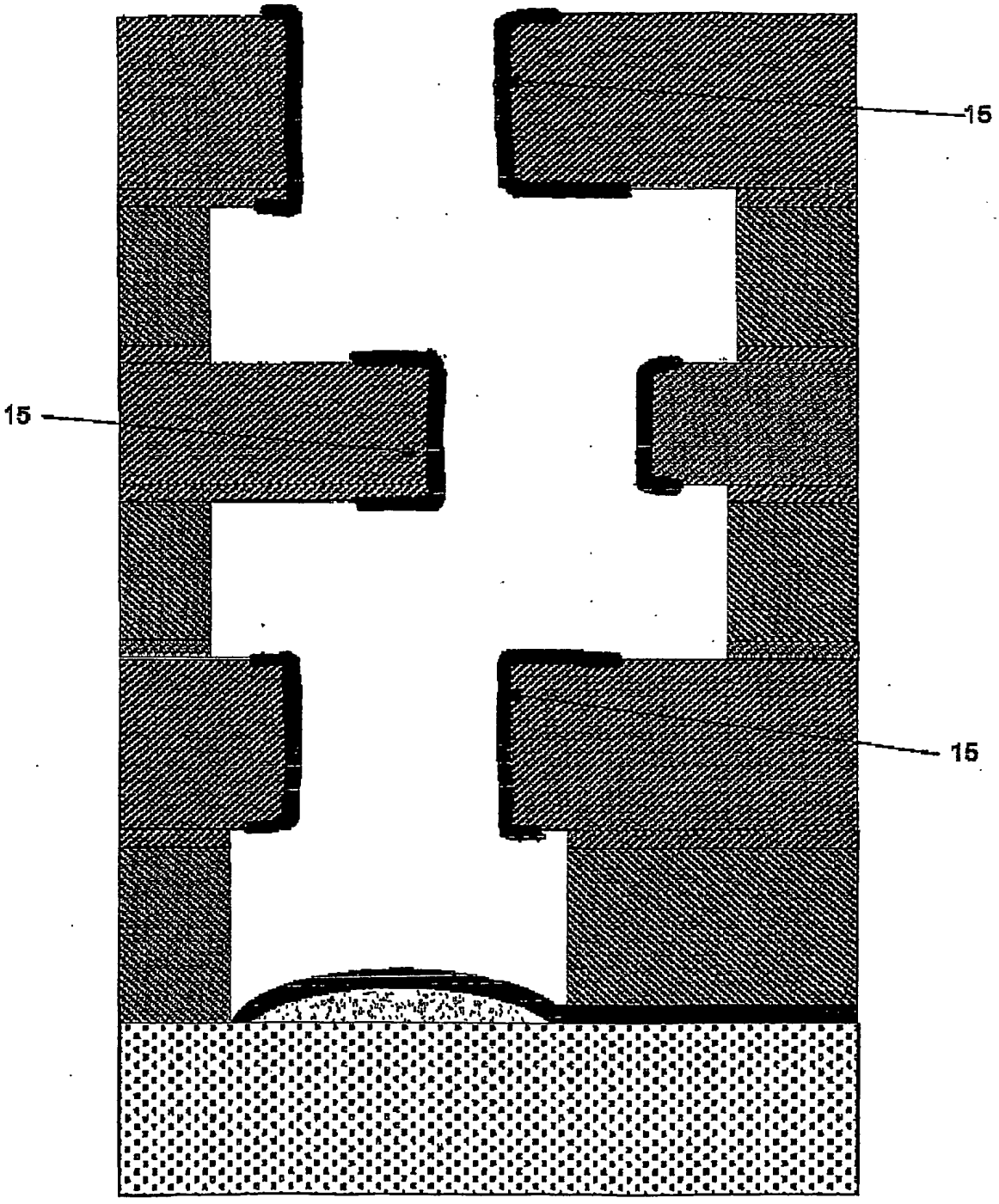

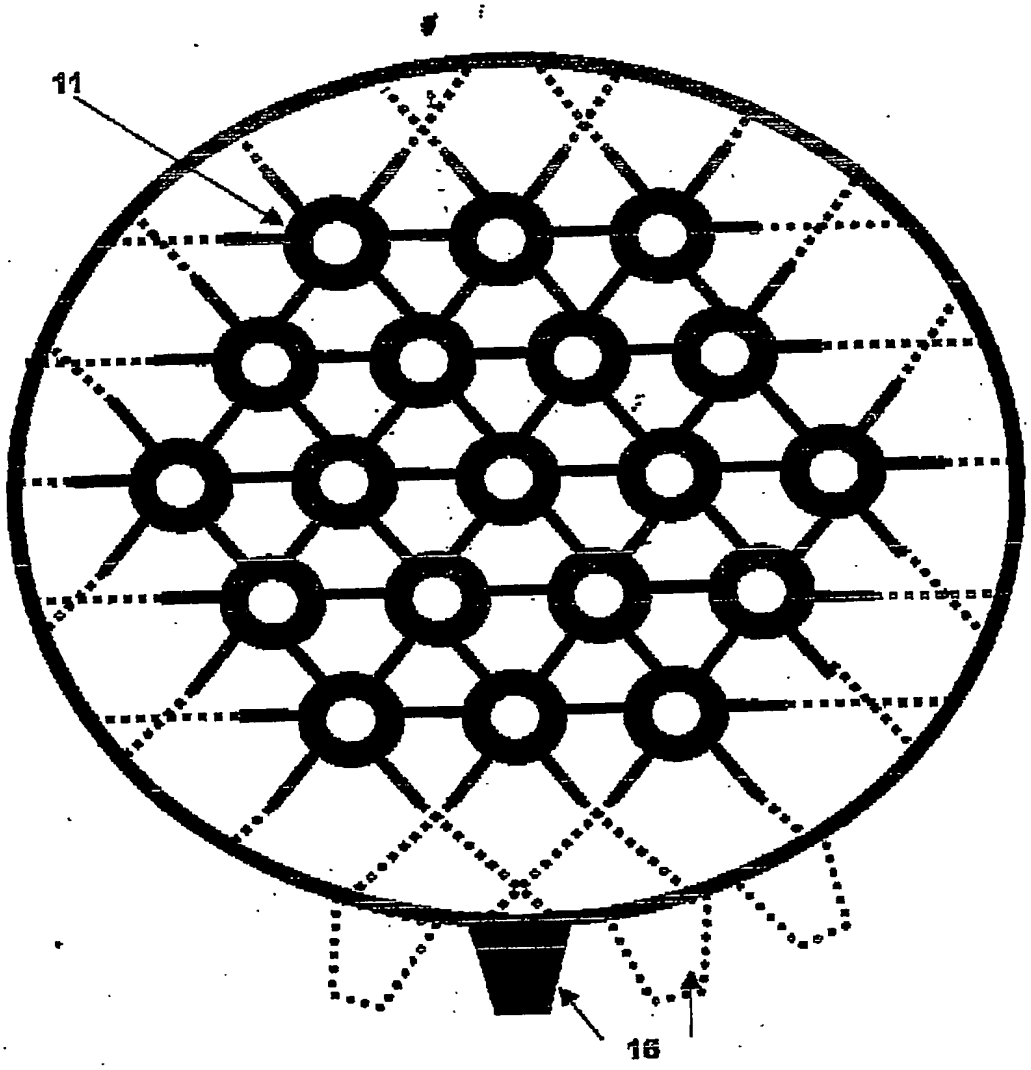

Fig. 3